# A Novel High-Gain DC-DC Converter Applied in Fuel Cell Vehicles 

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#### Abstract

The DC-DC converter for fuel cell vehicles should be characterized by high-gain, low voltage stress, small size and highefficiency. However, conventional two-level, three-level and cascaded boost converters cannot meet the requirements. A new non-isolated DC-DC converter with switched-capacitor and switched-inductor is proposed in this paper, which can obtain high-gain, wide input voltage range, low voltage stresses across components and common ground structure. In this paper, the operating principle, component parameters design, and comparisons with other high-gain converters are analyzed. Moreover, the state-space averaging method and small-signal modeling method are adopted to obtain the dynamic model of converter. Finally, simulation and experimental results verify the effectiveness of the proposed topology. The input voltage of the experimental prototype ranges from 25 V to 80 V . The rated output voltage is 200 V and rated power is 100 W . The maximum efficiency is $\mathbf{9 3 . 1 \%}$ under rated state. The proposed converter is suitable for fuel cell vehicles.


Index Terms-Fuel cell vehicles, DC-DC converter, switchedcapacitor and switched- inductor, high-gain, low voltage stress.

## I. Introduction

THE development of the transportation industry plays a vital role in the national economy. However, an increase in the number of fuel vehicles not only consumes a large amount of oil resources, but also causes serious environmental pollution problems. Therefore, all countries turn their attentions to the clean energy [1], [2]. The development of new energy vehicle industry provides new ideas to solve these problems. Fuel cell vehicle has become a very promising development direction in the new energy vehicle industry due to its advantages of zero emissions, no pollution and high efficiency [3], [4].

The typical system structure of fuel cell vehicle is shown in Fig. 1. The low output voltage of fuel cell makes it difficult to meet the demand of DC bus voltage in front of inverter. Moreover, the fuel cell has a "soft" output voltage characteristic, i.e., the output voltage drops too fast with the increase of the output current [5], [6]. Therefore, the DC-DC converter with high-gain, wide input voltage range and small size should be applied to fuel cell vehicles to raise the fuel cell voltage to a higher voltage level and ensure the stability of the DC bus voltage.

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Fig. 1. The typical system structure of fuel cell vehicle.
Isolated DC-DC converter can easily achieve high-gain by changing the transformer turns ratio. However, due to the leakage inductance of the transformer, the circuit will produce a peak voltage, which is easy to breakdown the devices in the circuit. The leakage inductance can also reduce the efficiency of the converter and cause electromagnetic interference problems. In addition, transformer in the isolated converter also increases the size of the converter [7], [8]. Considering the size, cost and efficiency, the non-isolated DC-DC converter is more suitable for fuel cell vehicles.

The traditional boost DC-DC converter is still used in many applications because of the small number of components and simple structure. The theoretical voltage gain of the boost converter is $1 /(1-d)$, where $d$ is the duty cycle of the drive voltage for power switch. However, the voltage gain is limited due to the parasitic parameters of the actual circuit and components. The voltage stresses across components in the circuit are also high, which needs more expensive high-voltage components, resulting in increased size and cost [9]. In addition, there is an extreme duty cycle in traditional boost converter when achieving high-gain, which causes serious diode reverse recovery problems, resulting in increased losses [10], [11]. In terms of these disadvantages, conventional boost converter is not suitable for fuel cell vehicles. The cascaded boost converter can achieve high-gain and wide input voltage range by sacrificing the overall power density and efficiency of converter, but the voltage stresses across components are high and the circuit structures are complex [12], [13]. The boost three-level DC-DC converter can reduce the voltage stresses across components, but the voltage gain is still as low as the conventional boost converter [14].

In [15], the voltage stresses across components are significantly reduced and the theoretical voltage gain can reach $(1+d) /(1-d)$, which is slightly larger than the conventional boost converter. However, the voltage gain in [15] is still not
enough for fuel cell vehicles. Z-source and quasi-Z-source networks are applied to the DC-DC converter to obtain the high-gain, but the voltage stresses of components in the converter are still high [16], [17]. In [18], a converter based on a series structure of three Z-source networks is proposed, which can obtain high-gain, wide input voltage range and low stress. However, there are too many inductors and power semiconductors in the circuit, which increases the cost and size of the converter. The converters proposed in [19]-[21] can achieve high-gain and low voltage stress, but there is a noncommon ground structure between the input and output ports of each converter. When the converter is working, there is a high frequency pulsated voltage between the input and output ports, which can cause serious EMI problems. In addition, the main problem is about the voltage feedback for the non-common ground structure. An isolated voltage feedback should be adopted, such as: linear optocoupler, which can increase the complexity of the sampling circuit [22]. The multi-level converters proposed in [23], [24] can achieve high-gain and low voltage stresses across components. However, there are too many power semiconductors in the the circuit, resulting in increased cost and size. Multiple power switches also increase complexity to the drive circuit and control strategy. The nonisolated converters with coupled-inductor proposed in [25]-[27] can easily achieve high-gain, reduce the size of inductor and increase the power density of the converter. However, due to the existence of leakage inductance, additional clamp circuit or absorption circuit should be adopted to absorb the leakage inductance energy, which increases the complexity of the converter.

In this paper, a DC-DC converter based on switchedcapacitor and switched-inductor is proposed. The converter can obtain high-gain, wide input voltage range, low voltage stress and common ground structure between input and output ports. In addition, there is no extreme duty cycle and the power switches need only one PWM drive signal in circuit topology. This paper is organized as follows: In Section II, the operating principle, voltage gain and voltage stresses across components are analyzed. And the converter is also compared with other high-gain DC-DC converters. In section III, the component parameters are designed. The dynamic model of the converter is presented by using state-space averaging method and smallsignal modeling method. In Section IV and Section V, the simulation and experimental results are presented respectively to verify the effectiveness of proposed converter. Finally, the conclusion is given in Section VI.

## II. Principle of the Proposed Converter

## A. Configuration of the Proposed Converter

The circuit topology of the proposed converter is shown in Fig. 2. $U_{\text {in }}$ and $U_{\mathrm{O}}$ are the input voltage and output voltage respectively. $R_{\mathrm{L}}$ is the load resistance. The converter consists of two power switches $\left(Q_{1}, Q_{2}\right)$, five diodes $\left(D_{1}-D_{5}\right)$, four capacitors $\left(C_{1}-C_{4}\right)$ and an inductor $L . Q_{1}$ and $Q_{2}$ are turned on and off simultaneously by using the same gate drive signal $S$.

When power switches $Q_{1}$ and $Q_{2}$ are turned on, $S=1$, and vice versa, calling $S=0$.


Fig. 2. The circuit topology of the proposed converter.

## B. Operating Principle of the Proposed Converter

In order to analyze the proposed converter topology, some assumptions are made as follow:
a) The forward voltage drop of diode and the on-state resistance of power switch are ignored. The equivalent series resistances of inductor and capacitors are equal to 0 .
b) The inductor is large enough in order to ensure that the circuit works normally. The capacitors are large enough in order to ensure that the voltage ripple of capacitors meets the requirements in this paper.

In this paper, the operating principle in Continuous Conduction Mode (CCM) is analyzed. The key operating waveforms of the proposed converter in CCM are shown in Fig. 3. According to the switching states of power switches, there are two operating states for the proposed converter, as shown in Fig. 4.


Fig. 3. The key operating waveforms of proposed converter in CCM.
When power switches $Q_{1}$ and $Q_{2}$ are turned on $(S=1)$, the equivalent circuit is shown in Fig. 4(a), defined as ON state. The diode $D_{1}, D_{2}, D_{3}, D_{5}$ are reverse biased and three current loops appear in the circuit. $U_{\text {in }}$ and $C_{1}$ charge the inductor $L$ through $Q_{1}$ and $Q_{2}$. Capacitor $C_{4}$ charges the capacitor $C_{2}$ through power switch $Q_{2}$ and diode $D_{4}$. The series part of the capacitors $C_{3}$ and $C_{4}$ transfers energy to the load $R_{\mathrm{L}}$.

When power switches $Q_{1}$ and $Q_{2}$ are turned off $(S=0)$, the equivalent circuit is shown in Fig. 4(b), defined as OFF state. The diode $D_{4}$ is reverse biased and four current loops appear in the circuit. Inductor $L$ charges capacitor $C_{1}$ through $D_{1}$ and $D_{2}$. $U_{\text {in }}$ and $L$ charge capacitor $C_{4}$ through $D_{1}$ and $D_{3} . U_{\text {in }}, L$ and $C_{2}$ charge the series part of $C_{3}$ and $C_{4}$ through the diodes $D_{1}$ and $D_{5}$. The series part of the capacitors $C_{3}$ and $C_{4}$ still transfers energy to the load $R_{\mathrm{L}}$.


Fig. 4. Two operating states of the proposed converter. (a) ON state. (b) OFF state.

## C. Analysis of Voltage Gain and Voltage Stress

Equations (1) and (2) can be obtained by applying Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) to the circuit topology in Fig. 4(a).

$$
\left\{\begin{array}{l}
U_{\mathrm{LON})}=U_{\mathrm{in}}+U_{\mathrm{C} 1}  \tag{1}\\
U_{\mathrm{C} 2}=U_{\mathrm{C} 4} \\
U_{\mathrm{O}}=U_{\mathrm{C} 3}+U_{\mathrm{C} 4}
\end{array}\right.
$$

where $U_{\mathrm{C} 1}, U_{\mathrm{C} 2}, U_{\mathrm{C} 3}$ and $U_{\mathrm{C} 4}$ are the capacitor voltages across $C_{1}, C_{2}, C_{3}$ and $C_{4}$ respectively. $U_{\mathrm{L}(\mathrm{ON})}$ is the inductor voltage across $L$ when the converter operates in ON state. $U_{\mathrm{O}}$ is the output voltage of the converter.

$$
\left\{\begin{array}{l}
I_{\mathrm{C} 1(\mathrm{ON})}=-I_{\mathrm{L}}  \tag{2}\\
I_{\mathrm{C} 2(\mathrm{ON})}=I_{\mathrm{C} 3(\mathrm{ON})}-I_{\mathrm{C} 4(\mathrm{ON})} \\
I_{\mathrm{C} 3(\mathrm{ON})}=-I_{\mathrm{O}}
\end{array}\right.
$$

where $I_{\mathrm{L}}$ is the average current of inductor $L . I_{\mathrm{C} 1(\mathrm{ON})}, I_{\mathrm{C} 2(\mathrm{ON})}$, $I_{\mathrm{C} 3(\mathrm{ON})}$, and $I_{\mathrm{C} 4(\mathrm{ON})}$ are the average currents of the capacitors $C_{1}$, $C_{2}, C_{3}$ and $C_{4}$ respectively, when the converter operates in ON state. $I_{O}$ is the load current.

Equations (3) and (4) can be obtained by applying KVL and KCL to the circuit topology in Fig. 4(b).

$$
\left\{\begin{array}{l}
U_{\mathrm{L}(\mathrm{OFF})}=-U_{\mathrm{C} 1}  \tag{3}\\
U_{\mathrm{C} 4}=U_{\mathrm{in}}-U_{\mathrm{L}(\mathrm{OFF})} \\
U_{\mathrm{o}}=U_{\text {in }}-U_{\mathrm{LOFF})}+U_{\mathrm{C} 2} \\
U_{\mathrm{O}}=U_{\mathrm{C} 3}+U_{\mathrm{C} 4}
\end{array}\right.
$$

where $U_{\text {L(OFF) }}$ is the the inductor voltage across $L$ when the converter operates in OFF state.

$$
\left\{\begin{array}{l}
I_{\mathrm{Cl}(\mathrm{OFF})}=I_{\mathrm{L}}+I_{\mathrm{C} 2(\mathrm{OFF})}+I_{\mathrm{C} 3(\mathrm{OFF})}-I_{\mathrm{C} 4(\mathrm{OFF})}  \tag{4}\\
I_{\mathrm{C} 2(\mathrm{OFF})}=-I_{\mathrm{O}}-I_{\mathrm{C} 3(\mathrm{OFF})}
\end{array}\right.
$$

where $I_{\mathrm{Cl}(\mathrm{OFF})}, I_{\mathrm{C} 2(\mathrm{OFF})}, I_{\mathrm{C} 3(\mathrm{OFF})}$, and $I_{\mathrm{C} 4(\mathrm{OFF})}$ are the average currents of the capacitors $C_{1}, C_{2}, C_{3}$ and $C_{4}$ respectively, when the converter operates in OFF state.

Equation (5) can be obtained by applying the voltage-second balance principle to inductor $L$, and equation (6) can be obtained by applying the ampere-second balance principle to capacitors $C_{1}, C_{2}, C_{3}$ and $C_{4}$.

$$
\begin{equation*}
U_{\mathrm{LON})} \times d T+U_{\mathrm{L}(\mathrm{OFF})} \times(1-d) T=0 \tag{5}
\end{equation*}
$$

$$
\left\{\begin{array}{l}
I_{\mathrm{C} 1(\mathrm{ON})} \times d T+I_{\mathrm{C} 1(\mathrm{OFF})} \times(1-d) T=0  \tag{6}\\
I_{\mathrm{C} 2(\mathrm{ON})} \times d T+I_{\mathrm{C} 2(\mathrm{OFF})} \times(1-d) T=0 \\
I_{\mathrm{C} 3(\mathrm{ON})} \times d T+I_{\mathrm{C} 3(\mathrm{OFF})} \times(1-d) T=0 \\
I_{\mathrm{C} 4(\mathrm{ON})} \times d T+I_{\mathrm{C} 4(\mathrm{OFF})} \times(1-d) T=0
\end{array}\right.
$$

where $d$ is duty cycle of power switches $Q_{1}$ and $Q_{2} . T$ is the switching period.

In terms of (1), (3) and (5), the theoretical voltage gain $M$ of the converter can be obtained as shown in (7).

$$
\begin{equation*}
M=\frac{U_{\mathrm{o}}}{U_{\mathrm{in}}}=\frac{2(1-d)}{1-2 d} \tag{7}
\end{equation*}
$$

where $0<d<0.5$. The proposed converter cannot work normally if $d>0.5$.

In terms of (1), (3), (5) and Fig. 4, the voltage stresses across all capacitors and power semiconductors in the circuit topology are obtained as shown in (8).

$$
\left\{\begin{array}{l}
U_{\mathrm{C} 1}=U_{\mathrm{D} 1}=U_{\mathrm{Q} 1}=U_{\mathrm{o}} / 2-U_{\mathrm{in}}  \tag{8}\\
U_{\mathrm{C} 2}=U_{\mathrm{C} 3}=U_{\mathrm{C} 4}=U_{\mathrm{o}} / 2 \\
U_{\mathrm{D} 2}=U_{\mathrm{D} 3}=U_{\mathrm{D} 4}=U_{\mathrm{D} 5}=U_{\mathrm{o}} / 2 \\
U_{\mathrm{Q} 2}=U_{\mathrm{o}} / 2
\end{array}\right.
$$

From (7), the converter can obtain a high-gain and the duty cycle $d$ is always less than 0.5 without extreme duty cycles. From (8), the voltage stresses of all capacitors and power semiconductors in the circuit topology are no more than $U_{\mathrm{O}} / 2$, which is beneficial to reducing size, cost and improving efficiency of the converter.

Assuming that the input power of the converter is equal to the output power in the ideal state, equation (9) can be obtained.

$$
\begin{equation*}
U_{\text {in }} \times I_{\text {in }}=U_{\mathrm{o}} \times I_{\mathrm{o}} \tag{9}
\end{equation*}
$$

where $I_{\mathrm{in}}$ is the average input current of the converter.
In terms of (2), (4), (6), (9) and Fig. 4, the inductor current $I_{\mathrm{L}}$ is obtained as shown in (10) and the current stresses of all capacitors in the circuit topology are obtained as shown in (11).

$$
\begin{equation*}
I_{\mathrm{L}}=\frac{2}{1-2 d} I_{\mathrm{O}} \tag{10}
\end{equation*}
$$

$$
\left\{\begin{array}{l}
I_{\mathrm{C} 1(\mathrm{ON})}=\frac{-2}{1-2 d} I_{\mathrm{o}}  \tag{11}\\
I_{\mathrm{C} 1(\mathrm{OFF})}=\frac{2 d}{(1-2 d)(1-d)} I_{\mathrm{O}} \\
I_{\mathrm{C} 2(\mathrm{ON})}=\frac{1}{d} I_{\mathrm{O}} \\
I_{\mathrm{C} 2(\mathrm{OFF})}=\frac{-1}{1-d} I_{\mathrm{O}} \\
I_{\mathrm{C} 3(\mathrm{ON})}=-I_{\mathrm{O}} \\
I_{\mathrm{C} 3(\mathrm{OFF})}=\frac{d}{1-d} I_{\mathrm{O}} \\
I_{\mathrm{C} 4(\mathrm{ON})}=-\left(1+\frac{1}{d}\right) I_{\mathrm{O}} \\
I_{\mathrm{C} 4(\mathrm{OFF})}=\frac{1+d}{1-d} I_{\mathrm{O}}
\end{array}\right.
$$

In terms of (10), (11) and Fig. 4, the current stresses of all power semiconductors are obtained as shown in (12).

$$
\left\{\begin{array}{l}
I_{\mathrm{Q} 1}=I_{\mathrm{D} 1}=-I_{\mathrm{C} 1(\mathrm{ON})}=\frac{2}{1-2 d} I_{\mathrm{o}}  \tag{12}\\
I_{\mathrm{Q} 2}=I_{\mathrm{L}}+I_{\mathrm{C} 2(\mathrm{ON})}=\frac{1}{d(1-2 d)} I_{\mathrm{o}} \\
I_{\mathrm{D} 2}=-I_{\mathrm{C} 1(\mathrm{OFF})}=\frac{-2 d}{(1-d)(1-2 d)} I_{\mathrm{O}} \\
I_{\mathrm{D} 3}=I_{\mathrm{C} 4(\mathrm{OFF})}-I_{\mathrm{C} 3(\mathrm{OFF})}=\frac{1}{1-d} I_{\mathrm{o}} \\
I_{\mathrm{D} 4}=I_{\mathrm{C} 2(\mathrm{ON})}=\frac{1}{d} I_{\mathrm{o}} \\
I_{\mathrm{D} 5}=I_{\mathrm{O}}+I_{\mathrm{C} 3(\mathrm{OFF})}=\frac{1}{1-d} I_{\mathrm{O}}
\end{array}\right.
$$

The MOSFET is adopted as power switch in experimental prototype of the proposed converter. Because the MOSFET and Schottky diode are suitable for low voltage and large current applications, this paper is only concerned with the voltage stresses of the components. The current stresses of the components are only used as an auxiliary reference for later component selection.

## D. Comparisons With Other Converters

The proposed converter is compared with other converters in terms of voltage gain, voltage stress, the number of components, and common ground structure, as shown in Table I. The relationships between voltage gain $M$ and duty cycle $d$ among different converters are shown in Fig. 5.

Compared with conventional boost converter, the proposed converter can obtain a higher gain. When the proposed converter achieves high-gain, the duty cycle is always less than 0.5 without extreme duty cycle. Furthermore, the voltage stresses across components of the proposed converter are no more than $U_{0} / 2$, rather than the $U_{\mathrm{O}}$ of conventional boost converter. The low voltage-stress can reduce the volume and cost of the capacitors, which occupy large volume of converter. The low voltage-stress can also reduce the voltage breakdown risk of the device and improve the reliability of the converter.

Two converters for fuel cell vehicles are proposed in [28] and [29] with low voltage stress and wide input voltage range. The voltage stresses across all components are reduced to $U_{\mathrm{O}} / 2$ and the voltage gain $(M=2 /(1-d))$ is two times better than the conventional boost converter. But the voltage gain is lower than that of the proposed converter in this paper, and these two converters may suffer from extreme duty cycles when high-gain is achieved. Furthermore, the circuit topologies are noncommon ground structure and there is a potential difference equal to $U_{\mathrm{O}} / 2$ between the input and output ports in each converter, which can cause safety problems. Although this potential difference is not a high frequency pulsated voltage, the non-common ground structure also bring difficulty to the sampling of the output voltage. The converter in [30] can obtain low voltage stresses across components and the operating range of $d$ is from 0.5 to 0.75 . However, the voltage gain is still low and there is an extra inductor in circuit topology compared with the proposed converter in this paper.


Fig. 5. Relationships between voltage gain $M$ and duty cycle $d$ among different converters.

Compared with the traditional quasi-Z-source converter $(M=1 /(1-2 d))$, the voltage gain of the proposed converter $(M=2(1-d) /(1-2 d))$ is always larger than that of the traditional quasi-Z-source converter within $0<d<0.5$ and the smaller $d$ is, the greater voltage gain difference is. The voltage stresses across components of the proposed converter are no more than $U_{\mathrm{O}} / 2$, rather than the $U_{\mathrm{O}}$ of quasi-Z-source converter. The voltage gain of the converter in [31] is slightly greater than that of the proposed converter within $0.33<d<0.5$ and is smaller than that of the proposed converter within $0<d \leqslant 0.33$. But the voltage gain of the proposed converter in this paper can meet the requirements of high-gain for fuel cell vehicles. In addition, the converter in [31] adopts a large number of inductors, which increase the size of the converter. The circuit topology is a noncommon ground structure in [31] and there is a high frequency pulsated voltage between the input and output ports, which results in EMI problem.

The proposed converter can obtain high-gain, low voltage stresses across components. The common ground structure of proposed converter can also avoid EMI problem. In addition, the power switches can be driven by only one PWM driving signal, which is beneficial to reducing the complexity of driving

TABLE I
COMPARISONS WITH OTHER CONVERTERS

| Converters | Voltage gain | Inductors | Capacitors | Power switches | Diodes | Voltage stresses across capacitors | Voltage stresses across diodes | Voltage stresses across power switches | Common ground structure |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Boost converter | $1 /(1-d)$ | 1 | 1 | 1 | 1 | $U_{\mathrm{O}}$ | $U_{\mathrm{O}}$ | $U_{\mathrm{O}}$ | Yes |
| Converter in [28] | $2 /(1-d)$ | 2 | 3 | 2 | 3 | $U_{0} / 2$ | $U_{0} / 2$ | $U_{0} / 2$ | No |
| Converter in [29] | $2 /(1-d)$ | 1 | 3 | 1 | 3 | $U_{0} / 2$ | $U_{0} / 2$ | $U_{\mathrm{O}} / 2$ | No |
| Converter in [30] | $2 /(3-4 d)$ | 2 | 4 | 3 | 4 | $\leq U_{0} / 2$ | $U_{0} / 2$ | $U_{0} / 2$ | Yes |
| Quasi-Z-converter | $1 /(1-2 d)$ | 2 | 3 | 1 | 2 | $U_{\mathrm{O}}$ | $U_{\mathrm{O}}$ | $U_{\mathrm{O}}$ | Yes |
| Converter in [31] | $(1+d) /(1-2 d)$ | 3 | 5 | 1 | 3 | $U_{\mathrm{O}} /(1+d)$ | $U_{0} /(1+d)$ | $U_{0} /(1+d)$ | No |
| Proposed converter | $2(1-d) /(1-2 d)$ | 1 | 4 | 2 | 5 | $\leq U_{0} / 2$ | $\leq U_{0} / 2$ | $\leq U_{0} / 2$ | Yes |

circuits. By using switched capacitor technique, there should be inrush current when the converter works at hard switching conditions. This problem can be suppressed by reducing the voltage differential between two capacitors, which can be achieved by increasing the switching frequency. Besides, softswitching technique can also effectively suppress the EMI and inrush current caused by switched capacitor technique. Based on the comparison results among different converters, the proposed converter in this paper is more advantageous in terms of high-gain, wide input voltage range, low voltage stress and common ground structure.

## III. Parameters Design and Dynamic Modeling

## A. Design of Inductor and Capacitors

In terms of the converter topology in Fig. 2, the inductor $L$ can be calculated by (13).

$$
\begin{equation*}
L=u_{\mathrm{L}} \frac{d t}{d i \mathrm{~L}} \tag{13}
\end{equation*}
$$

The maximum inductor current and the maximum duty ratio can be obtained when the input voltage is the lowest, that is $U_{\mathrm{in}}=25 \mathrm{~V}$ in proposed converter. Therefore, the inductor is designed when $U_{\text {in }}=25 \mathrm{~V}, U_{\mathrm{O}}=200 \mathrm{~V}, f=20 \mathrm{kHz}$ and $R_{\mathrm{L}}=400 \Omega$ in this paper. Assuming the current ripple of inductor $L$ is $\Delta I_{L}$, hence, the current ripple coefficient of inductor $L$ is $\gamma=\Delta I_{\mathrm{L}} / \mathrm{IL}_{\mathrm{L}}$. In order to avoid excessive inductor current ripple, the ripple rate of inductor current is set as $\gamma \leq 0.4$. When the converter operates in the ON state as shown in Fig. 4(a), $u_{\mathrm{L}}=u_{\mathrm{in}}+u_{\mathrm{cl}}$, $d t=d \times T=d / f$. In terms of (7), (10) and (13), the calculation equation of inductance can be obtained as (14).

$$
\begin{equation*}
L \geq \frac{d(1-2 d) R_{\mathrm{L}}}{4 \gamma f}=750 \mu \mathrm{H} \tag{14}
\end{equation*}
$$

where $f$ is the switching frequency of the converter and $d$ is the duty cycle of the drive signal for power switches $Q_{1}$ and $Q_{2}$.

When $R_{\mathrm{L}}=400 \Omega$ and $U_{\mathrm{O}}=200 \mathrm{~V}$, the output current $I_{\mathrm{O}}=U_{\mathrm{O}} /$ $R_{\mathrm{L}}=0.5 \mathrm{~A}$. According to (10), $I_{\mathrm{L}}=7.14 \mathrm{~A}$ can be obtained. When $U_{\text {in }}=25 \mathrm{~V}$ and $U_{\mathrm{O}}=200 \mathrm{~V}$, the peak value of inductor current $I_{L_{-} \text {peak }}$ is obtained as shown in (15).

$$
\begin{equation*}
I_{\mathrm{L}-\text { peak }}=I_{\mathrm{L}}+\frac{\Delta I}{2}=I_{\mathrm{L}}+\frac{I_{\mathrm{L}} \gamma}{2}=8.6 \mathrm{~A} \tag{15}
\end{equation*}
$$

The energy storage of the magnetic core is calculated as shown in (16).

$$
\begin{equation*}
L \cdot I_{\mathrm{L} \text { peak }}^{2}=0.8 \mathrm{mH} \times(8.6 \mathrm{~A})^{2}=59.2 \mathrm{mH} \cdot \mathrm{~A}^{2} \tag{16}
\end{equation*}
$$

Considering the flux density and price, the ferrosilicon aluminum magnetic core is adopted in this paper. By referring to magnetic core selection curves of Magnetics company for the iron-silica-aluminum, the 77438 magnetic core is selected for inductor design in this paper.

The capacitor $C$ can be calculated by (17). Assuming the voltage ripples of capacitors $C_{1}, C_{2}, C_{3}, C_{4}$ are $\Delta U_{C 1}, \Delta U_{C 2}$, $\Delta U_{C 3}, \Delta U_{C 4}$, respectively. In terms of (11) and (17), the calculation equation of capacitance can be obtained as (18).

$$
\begin{align*}
& C=i_{\mathrm{C}} \frac{d t}{d u \mathrm{C}}  \tag{17}\\
&\left\{\begin{aligned}
C_{1} & =\frac{2 d I_{\mathrm{o}}}{(1-2 d) \Delta U_{C 1} f} \\
C_{2} & =\frac{I_{\mathrm{o}}}{\Delta U_{C 2} f} \\
C_{3} & =\frac{d I_{\mathrm{o}}}{\Delta U_{C 3} f} \\
C_{4} & =\frac{(1+d) I_{\mathrm{o}}}{\Delta U_{C 4} f}
\end{aligned}\right. \tag{18}
\end{align*}
$$

## B. Dynamic Modeling Analysis

When the converter operates in the ON state, capacitors $C_{2}$ and $C_{4}$ are in parallel as shown in Fig. 4(a). The relationship between $C_{2}$ and $C_{4}$ is shown in (19), indicating that there is an invalid variable between $C_{2}$ and $C_{4}$.

$$
\begin{equation*}
C_{2} \frac{d u_{\mathrm{C} 2}}{d t}=-C_{4} \frac{d u_{\mathrm{C} 4}}{d t} \tag{19}
\end{equation*}
$$

In order to eliminate the invalid variable between $C_{2}$ and $C_{4}$, the series equivalent resistance $r_{1}$ is introduced into $C_{2}$ and $C_{4}$ loop and equation (19) can be written as (20).

$$
\begin{equation*}
C_{2} \frac{d u_{\mathrm{C} 2}}{d t}=-\frac{u_{\mathrm{C} 4}-u_{\mathrm{C} 2}}{r_{1}} \tag{20}
\end{equation*}
$$

where the $r_{1}$ is the equivalent series resistance in $C_{2}$ and $C_{4}$ loop, defined as $r_{1}=0.01 \Omega$.

When the converter operates in the OFF state, the series equivalent resistance $r_{2}=0.01 \Omega$ is adopted to eliminate the invalid variable of $C_{1}, C_{2}, C_{3}$ and $C_{4}$ loops as shown in Fig. 4(b). After adopting equivalent resistances $r_{1}$ and $r_{1}$, the equivalent circuit topology is as shown in Fig. 6.


$\tilde{u} \circ(t)=[0,0,0,1,1]\left[\tilde{\dot{L}}(t), \tilde{u} \mathrm{c}_{1}(t), \tilde{u} \mathrm{c}_{2}(t), \tilde{u} \mathrm{c}_{3}(t), \tilde{u} \mathrm{c}_{4}(t)\right]^{T}$

$$
\begin{equation*}
G_{d \rightarrow u o}(s)=\left.\frac{\tilde{u}_{\mathrm{o}}(s)}{\tilde{d}(s)}\right|_{\tilde{u}_{\mathrm{in}}(s)=0}=\frac{-1.225 \times 10^{9} s^{4}-2.61 \times 10^{14} s^{3}+4.341 \times 10^{19} s^{2}+1.522 \times 10^{24} s-1.103 \times 10^{22}}{s^{5}+6.689 \times 10^{5} s^{4}+1.266 \times 10^{11} s^{3}+1.112 \times 10^{16} s^{2}+4.511 \times 10^{20} s+1.3 \times 10^{20}} \tag{26}
\end{equation*}
$$



Fig. 6. Circuit topology after adopting equivalent resistances $r_{1}$ and $r_{2}$.
The state-space averaging method is used to model the converter in CCM. $u_{\text {in }}(t)$ is the input variable, $u 0(t)$ is the output variable and $d(t)$ is the control variable. $i_{\mathrm{L}}(t), u_{\mathrm{Cl}}(t)$, $u_{\mathrm{C} 2}(t), u_{\mathrm{C} 3}(t), u_{\mathrm{C} 4}(t)$ are the state variables of inductor $L$ and capacitors $C_{1}, C_{2}, C_{3}, C_{4}$ respectively. When the converter operates in the ON state and the working time is $d T$, the state space equation is obtained as (21). When the converter operates in the OFF state and the working time is $(1-d) T$, the state space equation is obtained as (22). In terms of (21) and (22), the statespace averaging equation over a switching period can be obtained as shown in (23). Equation (24) is obtained when all variables are written as the sum of DC and small signals components. By substituting (24) into (23) and removing the DC components, the small signal model of the converter is obtained as shown in (25).

$$
\left\{\begin{array}{l}
i_{\mathrm{L}}(t)=I_{\mathrm{L}}+\tilde{i}_{\mathrm{L}}(t)  \tag{24}\\
u_{\mathrm{C} 1}(t)=U_{\mathrm{C} 1}+\tilde{u}_{\mathrm{C} 1}(t) \\
u_{\mathrm{C} 2}(t)=U_{\mathrm{C} 2}+\tilde{u}_{\mathrm{C} 2}(t) \\
u_{\mathrm{C} 3}(t)=U_{\mathrm{C} 3}+\tilde{u}_{\mathrm{C} 3}(t) \\
u_{\mathrm{C} 4}(t)=U_{\mathrm{C} 4}+\tilde{u}_{\mathrm{C} 4}(t) \\
u_{\mathrm{in}}(t)=U_{\mathrm{in}}+\tilde{u}_{\mathrm{in}}(t) \\
u_{\mathrm{O}}(t)=U_{\mathrm{o}+}+\tilde{\mathrm{O}}^{2}(t) \\
d(t)=D+\tilde{d}(t)
\end{array}\right.
$$

where $I_{\mathrm{L}}, U_{\mathrm{C} 1}, U_{\mathrm{C} 2}, U_{\mathrm{C} 3}, U_{\mathrm{C} 4}, U_{\mathrm{in}}, U_{\mathrm{O}}, D$ are the DC steady-state components of the corresponding variables. $\tilde{i}_{\mathrm{L}}(t), \tilde{u}_{\mathrm{C} 1}(t)$, $\tilde{u}_{\mathrm{C} 2}(t), \tilde{u}_{\mathrm{C} 3}(t), \tilde{u}_{\mathrm{C} 4}(t), \tilde{u}_{\mathrm{in}}(t), \tilde{u}_{\mathrm{O}}(t), \tilde{d}(t)$ are the small signal components of the corresponding variables.

TABLE II
DESIGN PARAMETERS OF THE CONVERTER

| Parameters | Values |
| :---: | :---: |
| Rated power $P$ | 100 W |
| Input voltage $U_{\mathrm{in}}$ | $25 \mathrm{~V}-80 \mathrm{~V}$ |
| Rated output Voltage $U_{\mathrm{O}}$ | 200 V |
| Rated load resistance $R_{\mathrm{L}}$ | $400 \Omega$ |
| Switching frequency $f$ | 20 kHz |
| Inductor $L$ | $800 \mu \mathrm{H}$ |
| Capacitors $C_{1}, C_{2}, C_{3}, C_{4}$ | $470 \mu \mathrm{~F}$ |
| Power switches $Q_{1}, Q_{2}$ | IXTK102N30P |
| Diodes $D_{1}, D_{2}, D_{3}, D_{4}, D_{5}$ | DSEC60-03A |

The design parameters of the converter are shown in Table II. When $U_{\mathrm{in}}=25 \mathrm{~V}$ and $U_{\mathrm{O}}=200 \mathrm{~V}$, in terms of (25) and Table II, the transfer functions of control-to-output is obtained as shown in (26).

The dynamic model of proposed converter in (26) is written into the pole-zero form as shown in (27). In order to simplify analysis, the original model in (27) is reduced from 5 to 4 order to obtain the simplified model in (28). By appropriate pole-zero elimination method, the $\left(s+3.135 \times 10^{5}\right)$ in numerator and the $\left(s+4.283 \times 10^{5}\right)$ in denominator are eliminated in (27). The BODE diagram curves of (27) and (28) are shown in Figure 7. From Fig. 7, it can be seen that the original and simplified model curves are approximately the same. Therefore, the PI controller is designed based on (28).


Fig. 7. Bode diagram of the proposed converter.
The PI controller is designed in order to achieve stable operation for the converter system. The block diagram of the closed-loop control system for the converter is shown in Fig. 8. $G_{F B}(s)$ is the feedback network transfer function. The actual prototype adopts the Hall sensor to collect the output voltage. $G_{d \rightarrow u 0}(s)$ is the transfer function of converter from control to output. $G_{\mathrm{PI}(s)}$ is the transfer function of PI controller as shown in (29). The converter system can obtain good dynamic and static performance by using the PI controller.


Fig. 8. The block diagram of the closed-loop control system of the converter

$$
\begin{gather*}
G_{\text {ZPK }}(s)=\frac{-1.2247 \times 10^{9}\left(s+3.135 \times 10^{5}\right)\left(s-1.307 \times 10^{5}\right)\left(s+3.031 \times 10^{4}\right)(s-0.007247)}{\left(s+4.283 \times 10^{5}\right)\left(s+1.165 \times 10^{5}\right)(s+0.2883)\left(s^{2}+1.242 \times 10^{4} s+9.04 \times 10^{7}\right)}  \tag{27}\\
\hat{G}_{\text {ZRK }}(s)=\frac{-1.2247 \times 10^{9}\left(s-1.307 \times 10^{5}\right)\left(s+3.031 \times 10^{4}\right)(s-0.007247)}{\left(s+1.165 \times 10^{5}\right)(s+0.2883)\left(s^{2}+1.242 \times 10^{4} s+9.04 \times 10^{7}\right)} \tag{28}
\end{gather*}
$$

$$
\begin{equation*}
G_{\mathrm{PI}}(s)=K_{\mathrm{P}}+\frac{K_{\mathrm{I}}}{s} \tag{29}
\end{equation*}
$$

where the $K_{\mathrm{P}}$ is the proportional coefficient and $K_{\mathrm{I}}$ is the integral coefficient.

For this work, $K_{\mathrm{p}}=0.000008$ and $K_{\mathrm{I}}=0.000005$. By using PI controller, the Bode diagram of the converter closed-loop system is shown in Fig. 9. The phase margin of the closed-loop system is $53.7^{\circ}$, which indicates the system can achieve stable operation.


Fig. 9. The BODE diagram of closed-loop system for the converter.
In terms of practicality and stability, the bilinear transformation method is adopted to design the digital controller in this paper. By using bilinear transformation method, the relation between variable $s$ in $s$ domain and variable $z$ in $z$ domain is shown in (30) as follows [32].

$$
\begin{equation*}
s=\frac{2}{T_{\mathrm{s}}} \cdot \frac{z-1}{z+1} \tag{30}
\end{equation*}
$$

where $T_{\mathrm{s}}$ is the sampling period of discrete system. $T_{\mathrm{s}}=$ 0.00005 s in this paper.

In terms of (29) and (30) above, by using bilinear transformation method, the PI controller equation in $z$ domain is obtained as (31).

$$
\begin{equation*}
\frac{d(z)}{V \mathrm{e}(z)}=\frac{\left(K_{\mathrm{P}}+\frac{T_{\mathrm{s}}}{2} \cdot K_{\mathrm{I}}\right) \cdot z+\frac{T_{\mathrm{s}}}{2} \cdot K_{\mathrm{I}}-K_{\mathrm{P}}}{z-1} \tag{31}
\end{equation*}
$$

where $V \mathrm{e}(z)$ is the input error voltage of PI controller in $z$ domain. $d(z)$ is output duty cycle of PI controller in $z$ domain.

The values of $K_{\mathrm{I}}, K_{\mathrm{P}}$ and $T_{\mathrm{S}}$ above are substituted into equation (31) to obtain (32) as follows.

$$
\begin{equation*}
\frac{d(z)}{\operatorname{Ve}(z)}=\frac{8 \times 10^{-6}+7.99 \times 10^{-6} \cdot z^{-1}}{1-z^{-1}} \tag{32}
\end{equation*}
$$

Equation (32) is transformed into the difference equation as shown in (33), which is the expression of the discrete PI controller. According to (33), PI control program can be written in controller to realize closed-loop control and ensure the stability of the converter system.

$$
\begin{equation*}
d(k)=d(k-1)+8 \times 10^{-6} \cdot \operatorname{Ve}(k)+7.99 \times 10^{-6} \cdot \operatorname{Ve}(k-1) \tag{33}
\end{equation*}
$$

## IV. Simulation Results and Analysis

In order to verify the effectiveness of the proposed converter, a simulation model is built for the converter system and simulation parameters are shown in Table II. When the input voltage is $U_{\mathrm{in}}=25 \mathrm{~V}$ and the reference output voltage is set as $U_{o_{-} \text {ref }}=200 \mathrm{~V}$, the simulation results are shown in Fig. 10. From Fig. 10, the inductor current $I_{\mathrm{L}}$ is 7.5 A , which are consistent with the theoretical calculation result in (10). The output voltage $U_{0}$ has been stable at 200 V . The voltage stresses across all capacitors and power semiconductors are as follows: $U_{\mathrm{Q} 1}=U_{\mathrm{C} 1}=U_{\mathrm{D} 1} \approx 75 \mathrm{~V}, U_{\mathrm{Q} 2}=U_{\mathrm{C} 2}=U_{\mathrm{C} 3}=U_{\mathrm{C} 4}=U_{\mathrm{D} 2}=U_{\mathrm{D} 3}$ $=U_{\mathrm{D} 4}=U_{\mathrm{D} 5} \approx 100 \mathrm{~V}$, which are consistent with the theoretical calculation results obtained in (8). The simulation results show that the proposed converter has advantages of high-gain and low voltage stresses across components, which verifies the effectiveness of the circuit topology.
The dynamic simulation results of the converter are shown in Figure 11. When the simulation time is 1 s , the input voltage of the converter $U_{\text {in }}$ starts to drop from 60 V and finally drops to 25 V , with a total time of 14 s . When the simulation time is 16 s , the output current $I_{\mathrm{O}}$ changes suddenly from 250 mA to 500 mA and remains 200 ms . Then the $I_{\mathrm{O}}$ changes suddenly from 500 mA to 250 mA . From Fig. 11, it can be concluded that the converter can maintain the output voltage stable around the reference voltage under the input voltage and load disturbance. The system can obtain a good anti-interference performance.


Fig. 10. Simulation results of converter. (a) Drive voltage $U_{\mathrm{gs}}$, inductor current $I_{\mathrm{L}}$, output voltage $U_{\mathrm{O}}$ and voltage stresses across $C_{1}, C_{2}, C_{3}, C_{4}$. (b) Drive voltage $U \mathrm{gs}$, voltage stresses across $Q_{1}, ~ Q_{2}$, voltage stresses across $D_{1}$, $D_{2}, D_{3}, D_{4}, D_{5}$.


Fig. 11. Simulation results of the converter under the input voltage disturbance and load disturbance.

## V. EXPERIMENTAL RESULTS AND ANALYSIS

The experimental prototype is built based on the circuit topology shown in Fig. 2 to verify the accuracy of theoretical calculation and simulation results. The design parameters of the prototype are shown in Table II. The main controller adopts the TMS320F28335 and the sampling circuits of voltage and current adopt Hall sensors. The experimental prototype is shown in Fig. 12 and the experimental test platform is shown in Fig. 13.


Fig. 12. Experimental prototype


Fig. 13. Experimental test platform
When the input voltage is $U_{\mathrm{in}}=25 \mathrm{~V}$ and the reference output voltage is set as $U_{\mathrm{O}_{-} \text {ref }}=150 \mathrm{~V}$, the experimental results are shown in Fig. 14. Fig. 14(a) shows the waveforms of drive voltage $U$ gs, inductor current $I_{\mathrm{L}}$ and output voltage $U_{\mathrm{O}}$. From Fig. 14(a), it can be seen that the switching frequency of the converter is 20 kHz and the duty cycle is $d \approx 0.4$. When power switches $Q_{1}$ and $Q_{2}$ are turned on, inductor $L$ is charged and inductor current $I_{\mathrm{L}}$ increases linearly. When $Q_{1}$ and $Q_{2}$ are turned off, inductor $L$ discharges and inductor current $I_{\mathrm{L}}$ decreases linearly. The output voltage $U_{\mathrm{O}}$ of the converter has been stable at the reference value of 150 V . The voltage stresses of all capacitors and power semiconductors are shown in Fig. 14(b)-Fig. 14(e). From these figures, it can be seen that $U_{\mathrm{Q} 1}=52$
$\mathrm{V}, U_{\mathrm{C} 1}=50 \mathrm{~V}$ and $U_{\mathrm{D} 1}=50 \mathrm{~V}$, which are basically consistent with the theoretical calculation result of 50 V obtained in (8). The voltage stresses across other capacitors and power semiconductors are as follows: $U_{\mathrm{Q} 2}=77 \mathrm{~V}, U_{\mathrm{C} 2}=72 \mathrm{~V}, U_{\mathrm{C} 3}=75$ $\mathrm{V}, U_{\mathrm{C} 4}=75 \mathrm{~V}, U_{\mathrm{D} 2}=75 \mathrm{~V}, U_{\mathrm{D} 3}=75 \mathrm{~V}, U_{\mathrm{D} 4}=77 \mathrm{~V}$ and $U_{\mathrm{D} 5}=75 \mathrm{~V}$, which are basically consistent with the theoretical calculation result of 75 V obtained in (8).


Fig. 14. Experimental waveforms when $U_{\mathrm{O}_{-} \text {ref }}=150 \mathrm{~V}$. (a) Drive voltage $U_{\mathrm{gs}}$, inductor current $I_{\mathrm{L}}$, output voltage $U_{\mathrm{O}}$. (b) Voltage stresses across $Q_{1}, Q_{2}, C_{1}$. (c) Voltage stresses across $C_{2}, C_{3}, C_{4}$. (d) Voltage stresses across $D_{1}, D_{2}, D_{3}$. (e) Voltage stresses across $D_{4}, D_{5}$.

The experimental waveforms are shown in Fig. 15 when the the reference output voltage of the closed-loop system is set as 200 V and the input voltage still remains at 25 V. Similar to Fig.

14, it can be seen from Fig. 15(a) that the switching frequency of the converter is 20 kHz , and the inductor current increases and decreases linearly.

The output voltage $U_{\mathrm{O}}$ of the converter has been stable at the reference value of 200 V . When the closed-loop system is stabilized, the duty cycle of the driving voltage is $d \approx 0.44$, which is slightly higher than the theoretical duty cycle $d=0.428$ obtained in (7). The voltage gain error between actual and the ideal states is caused by the parasitic parameters of the actual components.

When the actual output voltage is less than the reference value, the closed-loop system automatically raises the duty cycle of the driving voltage to increase the output voltage.

From Fig. 15(b)-Fig. 15(e), it can be seen that $U_{\mathrm{Q} 1}=75 \mathrm{~V}$, $U_{\mathrm{C} 1}=72 \mathrm{~V}, U_{\mathrm{D} 1}=72 \mathrm{~V}$, which are basically consistent with the theoretical calculation results of 75 V obtained in (8). The voltage stresses across other capacitors and power semiconductors are as follows: $U_{\mathrm{Q} 2}=100 \mathrm{~V}, U_{\mathrm{C} 2}=98 \mathrm{~V}$, $U_{\mathrm{C} 3}=100 \mathrm{~V}, U_{\mathrm{C} 4}=100 \mathrm{~V}, U_{\mathrm{D} 2}=100 \mathrm{~V}, U_{\mathrm{D} 3}=100 \mathrm{~V}, U_{\mathrm{D} 4}=102 \mathrm{~V}$ and $U_{\mathrm{D} 5}=99 \mathrm{~V}$, which are basically consistent with the theoretical calculation results of 100 V obtained in (8).

(b)

(c)

(d)


Fig. 15. Experimental waveforms when $U_{\mathrm{O} \text { _ref }}=200 \mathrm{~V}$. (a) Drive voltage $U_{\mathrm{gs}}$, inductor current $I_{\mathrm{L}}$, output voltage $U_{\mathrm{O}}$. (b) Voltage stresses across $Q_{1}, Q_{2}, C_{1}$.
(c) Voltage stresses across $C_{2}, C_{3}, C_{4}$. (d) Voltage stresses across $D_{1}, D_{2}, D_{3}$.
(e) Voltage stresses across $D_{4}, D_{5}$.

The above experimental results verify the effectiveness of the topology and the stability of the closed-loop control system. The converter has high-gain and the measured voltage stresses of the components are no more than $U_{\mathrm{O}} / 2$, which is beneficial to reduce the cost, size and improve the efficiency.

In order to validate the feature of wide input range, the DC high-power supply changes like a fuel cell source to simulate the "soft" output voltage characteristics of the fuel cell. The input voltage of the converter changes from 60 V to 25 V over 13.5 s , rather than a step change, when the reference output voltage is set at $U_{\text {O_ref }}=200 \mathrm{~V}$. The experimental waveforms are shown in Fig. 16. From Fig. 16, with the change of input voltage, the output voltage of the converter can keep stable around the reference voltage 200 V .


Fig. 16. The output voltage $U_{\mathrm{O}}$ and input voltage $U_{\text {in }}$ waveforms when the input voltage drops.

When the input voltage is $U_{\mathrm{in}}=25 \mathrm{~V}$ and the reference output voltage is set as $U_{\text {O_ref }}=200 \mathrm{~V}$, the load disturbance experimental results are shown in Fig. 17. When the load resistance changes between $400 \Omega$ and $800 \Omega$, the output voltage fluctuation is small and converter has a good closedloop control effect.


Fig. 17. Output voltage $U_{\mathrm{O}}$ and output current $I_{\mathrm{O}}$ waveforms under load disturbance

Voltage overshoot and impulse current may occur when the converter is started, which can damage the devices in circuit. In order to avoid the impulse current and voltage during the initial startup instant, a soft-start program is adopted in the controller to make the duty cycle slowly increase from 0 to the desired value. The soft-start time of the experimental prototype is set as

600 ms . When the input voltage is $U_{\mathrm{in}}=25 \mathrm{~V}$ and the reference output voltage is set as $U_{O_{-} \text {ref }}=200 \mathrm{~V}$, the experimental waveforms during soft-start process are shown in Fig. 18. In (7), the initial voltage gain of converter is already greater than 2 times when duty cycle $d$ is approximately 0 . Therefore, the output voltage $U_{\mathrm{O}}$, voltages across capacitors and inductor current all have small step changes at the beginning of soft-start in Fig. 18, instead of slowly increasing from zero. Although the small step changes are inevitable, there are not voltage overshoot and impulse current during the whole soft-start process.


Fig. 18. The experimental waveforms of the converter during soft-start process. (a) Output voltage $U_{\mathrm{O}}$. (b) Voltage stresses across $C_{1}$ and inductor current $I_{\mathrm{L}}$. (c) Voltage stresses across $C_{2}, C_{3}$ and $C_{4}$.

The efficiency test experiment is carried out, when the reference output voltage is set as $U_{\mathrm{O}_{-} \text {ref }}=200 \mathrm{~V}$ and the input voltage of the converter slowly changes from 30 V to 60 V . The efficiency curves of the prototype are shown Fig. 19. The measured maximum efficiency is $93.1 \%$ when the output power is 100 W . When the output power are 80 W and 50 W , the maximum measured efficiencies are $93.8 \%$ and $95.4 \%$ respectively.

When the output voltage is fixed, the greater the output power, the greater the total loss power. But whether the efficiency is decreasing all the time depends on the increase of the total loss power and the increase of the total output power. In Fig. 19, when $U_{\text {in }}=40 \mathrm{~V}$, the total loss power of the $P_{\text {out }}=80 \mathrm{~W}$ is 11 W and the corresponding efficiency is $87.9 \%$. When $U_{\text {in }}=40 \mathrm{~V}$, the total loss power of the $P_{\text {out }}=100 \mathrm{~W}$ is 13 W and the corresponding efficiency is $88.5 \%$. Although the total loss power of 100 W is higher than that of 80 W , the increase amplitude of the total loss power is low. Therefore, the efficiency of 100 W is slightly higher than that of 80 W .


Fig. 19. Converter efficiency curves when the output power are $100 \mathrm{~W}, 80 \mathrm{~W}$ and 50 W respectively.

## VI. CONCLUSION

This paper presents a non-isolated DC-DC converter topology for fuel cell vehicles. The proposed converter can obtain high-gain and wide input voltage range. The voltage gain can reach $2(1-d) /(1-2 d)$ and duty cycle $d<0.5$ while achieving high-gain. The voltage stresses across components are less than half of the output voltage, which is beneficial to reduce the size and cost of the converter. In addition, the circuit topology is a common ground structure, which can avoid EMI and safety problems. The converter can always maintain the stability of the output voltage by closed-loop control. There are not the voltage overshoot and impulse current during soft-start process by adopting the soft-start program. Under the rated state, the measured maximum efficiency of the prototype is $93.1 \%$. The proposed converter is suitable for fuel cell vehicles.

## REFERENCES

[1] G. Du, W. Cao, S. Hu, Z. Lin, and T. Yuan, "Design and Assessment of an Electric Vehicle Powertrain Model Based on Real-World Driving and Charging Cycles," IEEE Trans. Veh. Technol., vol. 68, no. 2, pp. 1178-1187, Feb. 2019.
[2] Z. Geng, Q. Chen, Q. Xia, D. S. Kirschen, and C. Kang, "Environmental Generation Scheduling Considering Air Pollution Control Technologies and Weather Effects," IEEE Trans. Power Syst., vol. 32, no. 1, pp. 127-136, Jan. 2017.
[3] H. Bi, P. Wang, and Y. Che, "A Capacitor Clamped H-Type Boost DCDC Converter With Wide Voltage-Gain Range for Fuel Cell Vehicles," IEEE Trans. Veh. Technol., vol. 68, no. 1, pp. 276-290, Jan. 2019.
[4] L. Li, S. Coskun, F. Zhang, R. Langari, and J. Xi, "Energy Management of Hybrid Electric Vehicle Using Vehicle Lateral Dynamic in Velocity Prediction," IEEE Trans. Veh. Technol., vol. 68, no. 4, pp. 3279-3293, Apr. 2019.
[5] N. Elsayad, H. Moradisizkoohi, and O. A. Mohammed, "A SingleSwitch Transformerless DC-DC Converter With Universal Input Voltage for Fuel Cell Vehicles: Analysis and Design," IEEE Trans. Veh. Technol., vol. 68, no. 5, pp. 4537-4549, Mar. 2019.
[6] O. Hegazy, J. Van Mierlo, and P. Lataire, "Analysis, Modeling, and Implementation of a Multidevice Interleaved DC-DC Converter for Fuel Cell Hybrid Electric Vehicles," IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4445-4458, Nov. 2012.
[7] Z. Qun and F. C. Lee, "High-efficiency, high step-up DC-DC converters," IEEE Trans. Power Electron., vol. 18, no. 1, pp. 65-73, Jan. 2003.
[8] B. Gu, J. Dominic, J.-S. Lai, Z. Zhao, and C. Liu, "High Boost Ratio Hybrid Transformer DC-DC Converter for Photovoltaic Module Applications," IEEE Trans. Power Electron., vol. 28, no. 4, pp. 20482058, Apr. 2013.
[9] C. T. Pan and C. M. Lai, "A High-Efficiency High Step-Up Converter With Low Switch Voltage Stress for Fuel-Cell System Applications," IEEE Trans. Ind. Electron., vol. 57, no. 6, pp. 1998-2006, Jun. 2010.
[10] G. A. L. Henn, R. N. A. L. Silva, P. P. Praça, L. H. S. C. Barreto, and D. S. Oliveira, "Interleaved-Boost Converter With High Voltage Gain,"

IEEE Trans. Power Electron., vol. 25, no. 11, pp. 2753-2761, Nov. 2010.
[11] F. Wen, J. Shabani, and E. Tutuc, "Josephson Junction Field-Effect Transistors for Boolean Logic Cryogenic Applications," IEEE Trans. Electron Devices., vol. 66, no. 12, pp. 5367-5374, Dec. 2019.
[12] F. L. Tofoli, D. de Castro Pereira; W. J. de Paula, and D. de Sousa Oliveira Junior, "Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter," IET Power Electron., vol. 8, no. 10, pp. 2044-2057, Sep. 2015.
[13] F. L. Luo and H. Ye, "Positive output cascade boost converters," in Proc. IEE Proc. Electr. Power Appl., vol. 151, no. 5, pp. 590-606, Sep. 2004.
[14] J. P. Rodrigues, S. A. Mussa, M. L. Heldwein, and A. J. Perin, "ThreeLevel ZVS Active Clamping PWM for the DC-DC Buck Converter," IEEE Trans. Power Electron., vol. 24, no. 10, pp. 2249-2258, Oct. 2009.
[15] Y. L. Sheng, L. T. Juu, and C. J. Fuh, "Transformerless DC-DC Converters With High Step-Up Voltage Gain," IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 3144-3152, Aug. 2009.
[16] J. Anderson and F. Z. Peng, "A Class of Quasi-Z-Source Inverters," in Proc. IEEE Ind. Appl. Soc., Oct. 2008, pp. 1-7.
[17] V. P. Galigekere and M. K. Kazimierczuk, "Analysis of PWM Z-Source DC-DC Converter in CCM for Steady State," IEEE Trans. Circuits Syst. I, Reg. Papers., vol. 59, no. 4, pp. 854-863, Apr. 2012.
[18] G. Zhang, B. Zhang, Z. Li, and D. Qiu, "A 3-Z-Network Boost Converter," IEEE Trans. Ind. Electron., vol. 62, no. 1, pp. 278-288, Jan. 2015.
[19] M. K. Nguyen, T. D. Duong, and Y. C. Lim, "Switched-CapacitorBased Dual-Switch High-Boost DC-DC Converter," IEEE Trans. Power Electron., vol. 33, no. 5, pp. 4181-4189, May. 2018.
[20] R. J. K. Prasana, S. Ramprasath, and N. Vijayasarathi, "Design and analysis of hybrid DC-DC boost converter in continuous conduction mode," in Proc. IEEE Int. Conf. Circuit, Power Comput. Technol., Power and Computing Technol., Mar. 2016, pp. 1-5.
[21] X. Hu and C. Gong, "A High Gain Input-Parallel Output-Series DC/DC Converter With Dual Coupled Inductors," IEEE Trans. Power Electron., vol. 30, no. 3, pp. 1306-1317, Mar. 2015.
[22] A. Rajaei, R. Khazan, M. Mahmoudian, and M. Mardaneh, "A Dual Inductor High Step-Up DC/DC Converter Based on the CockcroftWalton Multiplier," IEEE Trans. Power Electron., vol. 33, no. 11, pp. 9699-9709, Nov. 2018.
[23] X. B. Ruan, B. Li, Q. H. Chen, T. Siew-Chong, and C. K. Tse, "Fundamental Considerations of Three-Level DC-DC Converters: Topologies, Analyses, and Control," IEEE Trans. Circuits Syst. I, Reg. Papers., vol. 55, no. 11, pp. 3733-3743, Dec. 2008.
[24] L. Sun, F. Zhuo, F. Wang, and T. Zhu, "A novel topology of high voltage and high power bidirectional ZCS DC-DC converter based on serial capacitors," in Proc. IEEE Appl Power Electron Conf Expo APEC, Mar. 2016, pp. 810-815.
[25] J. H. Lee, T. J. Liang, and J. F. Chen, "Isolated Coupled-InductorIntegrated DC-DC Converter With Nondissipative Snubber for Solar Energy Applications," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3337-3348, Jul. 2014.
[26] C. S. Kuen, L. T. Juu, C. J. Fuh, and Y. L. Sheng, "Novel High StepUp DC-DC Converter for Fuel Cell Energy Conversion System," IEEE Trans. Ind. Electron., vol. 57, no. 6, pp. 2007-2017, Jun. 2010.
[27] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "A Novel High Step-Up DC-DC Converter for a Microgrid System," IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1127-1136, Apr. 2011.
[28] P. Wang, L. Zhou, Y. Zhang, J. Li, and M. Sumner, "Input-Parallel Output-Series DC-DC Boost Converter With a Wide Input Voltage Range, For Fuel Cell Vehicles," IEEE Trans. Veh. Technol., vol. 66, no. 9, pp. 7771-7781, Sep. 2017.
[29] Y. Zhang, L. Zhou, M. Sumner, and P. Wang, "Single-Switch, Wide Voltage-Gain Range, Boost DC-DC Converter for Fuel Cell Vehicles," IEEE Trans. Veh. Technol., vol. 67, no. 1, pp. 134-145, Jan. 2018.
[30] Y. Zhang, J. Shi, L. Zhou, and J Li, "Wide Input-Voltage Range Boost Three-Level DC-DC Converter With Quasi-Z Source for Fuel Cell Vehicles," IEEE Trans. Power Electron., vol. 32, no. 9, pp. 6728-6738, Sep. 2017.
[31] Y. Shindo, M. Yamanaka, and H. Koizumi, "Z-source DC-DC converter with cascade switched capacitor," in Proc. IEEE Ind. Electron. Soc., Nov. 2011, pp. 1665-1670.
[32] A. Narayana, "State-space approach to the bilinear transformation and some extensions," IEEE Trans. Educ., vol. 34, no. 1, pp. 139-142, Feb. 1991.


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